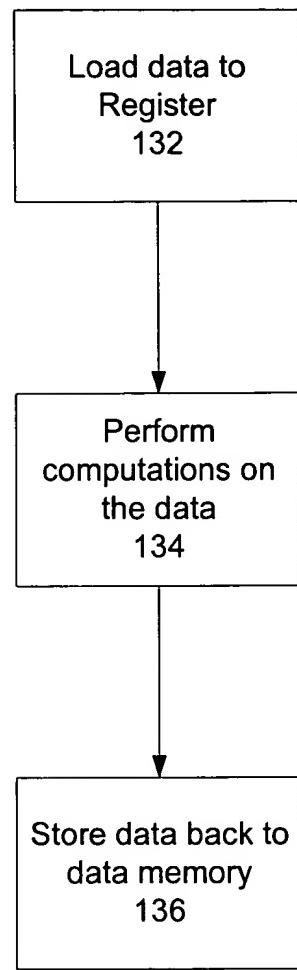


Figure 1A



053883295 - 07522034

Figure 1B

OPCode 6 bits	Source1 Register 5 bits	Source2 Register 5 bits	Target Register 5 bits	Sub-OPCode 11 bits
------------------	-------------------------------	-------------------------------	------------------------------	-----------------------

Figure 1C

00

OPCode 6 bits	Target Register 5 bits	Source1 Register 5 bits	Immediate 16 bits
------------------	------------------------------	-------------------------------	----------------------

Figure 1D

200

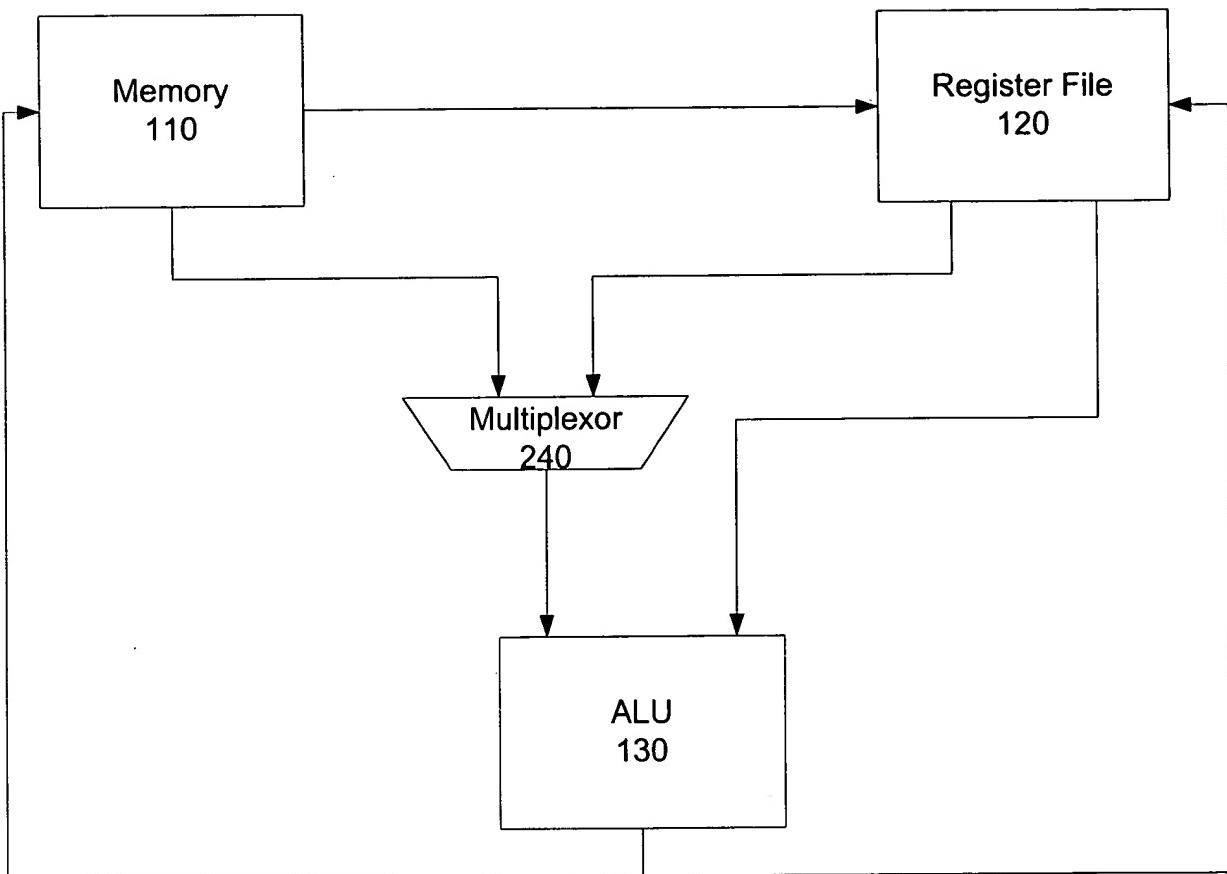


Figure 2

CODES2000-CODE2001

300

00000000 - 00000001

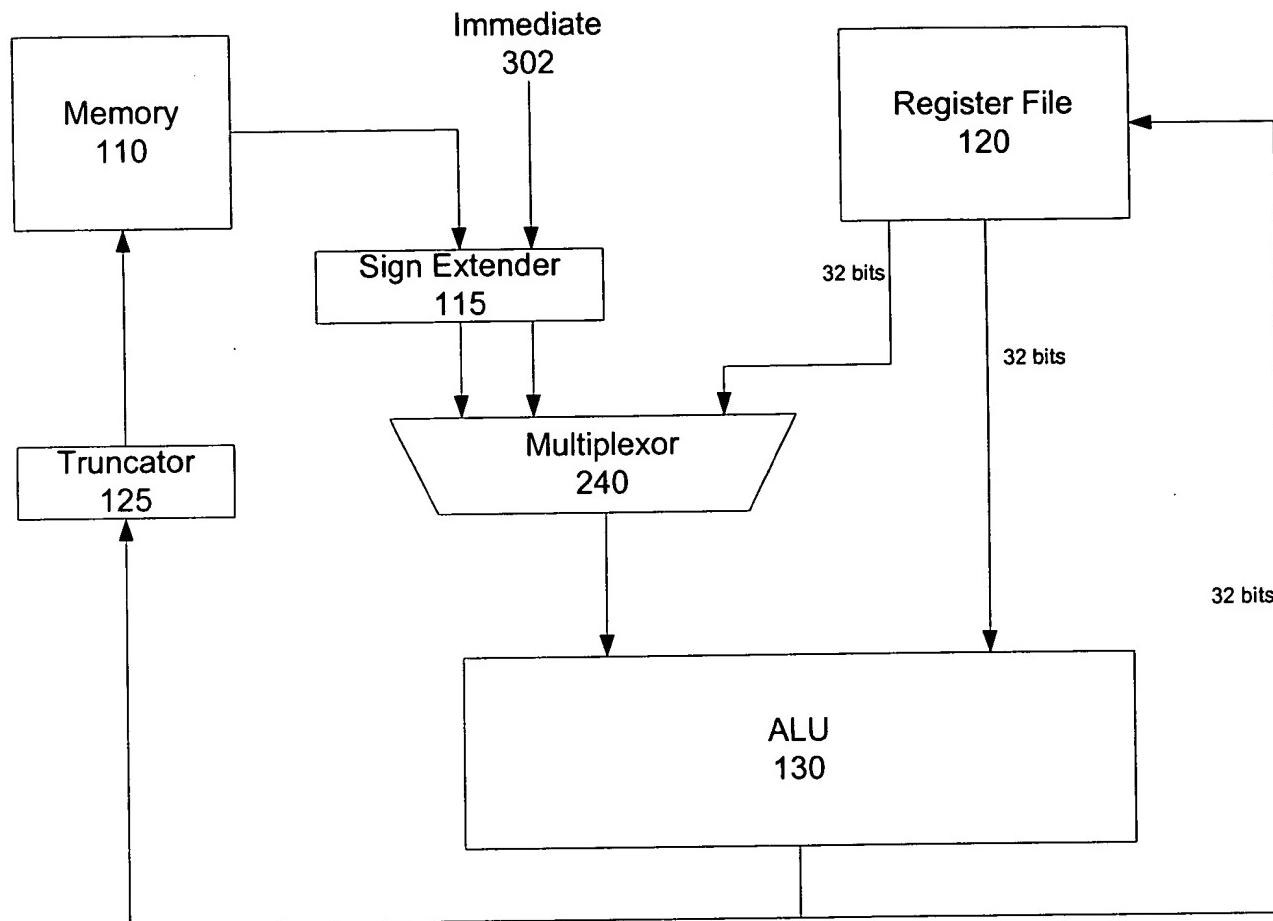


Figure 3A

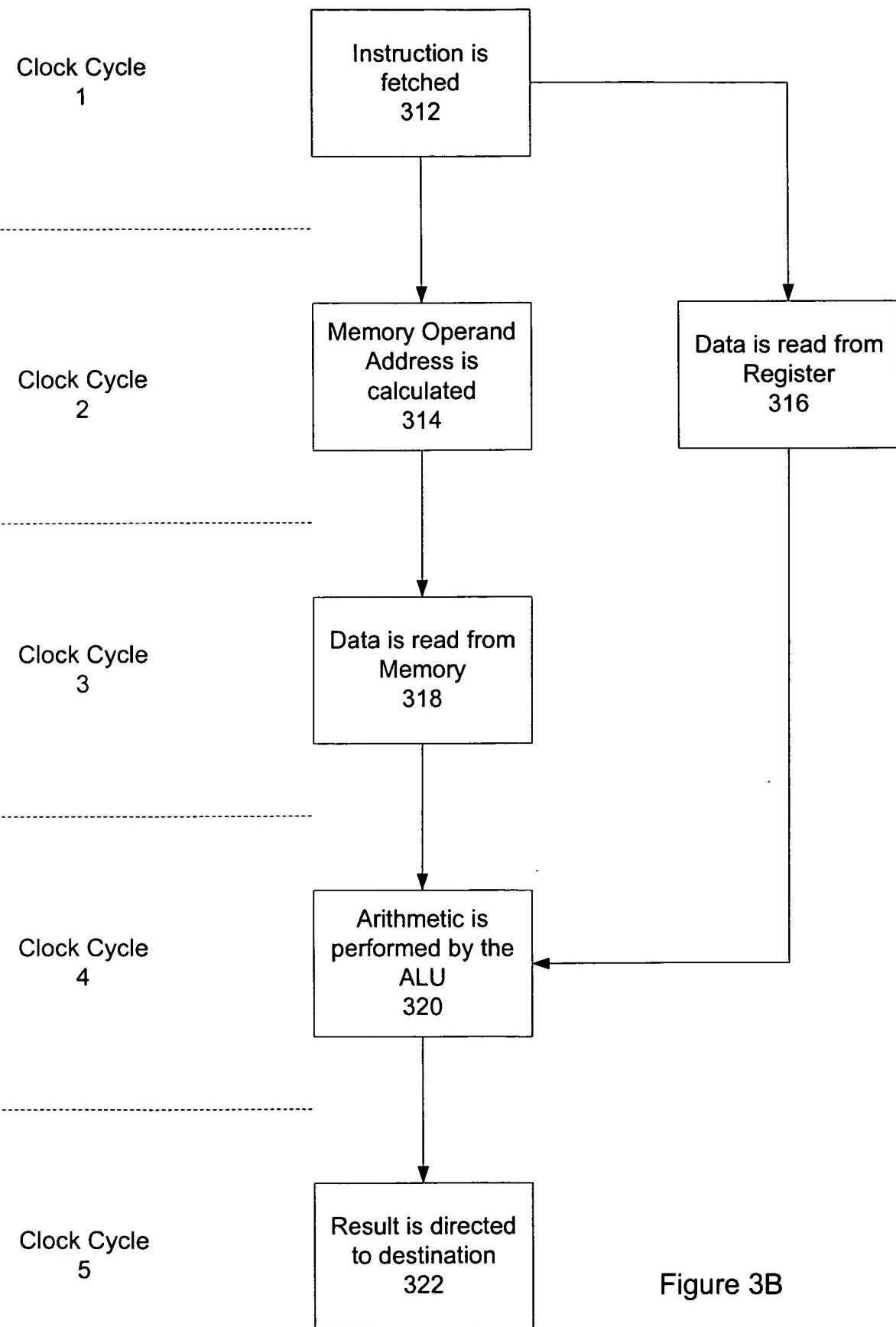


Figure 3B

400

OPCode 5 bits	Destination 11 bits	Source2 Register 5 bits	Source1 11 bits
------------------	------------------------	-------------------------------	--------------------

**Figure 4**

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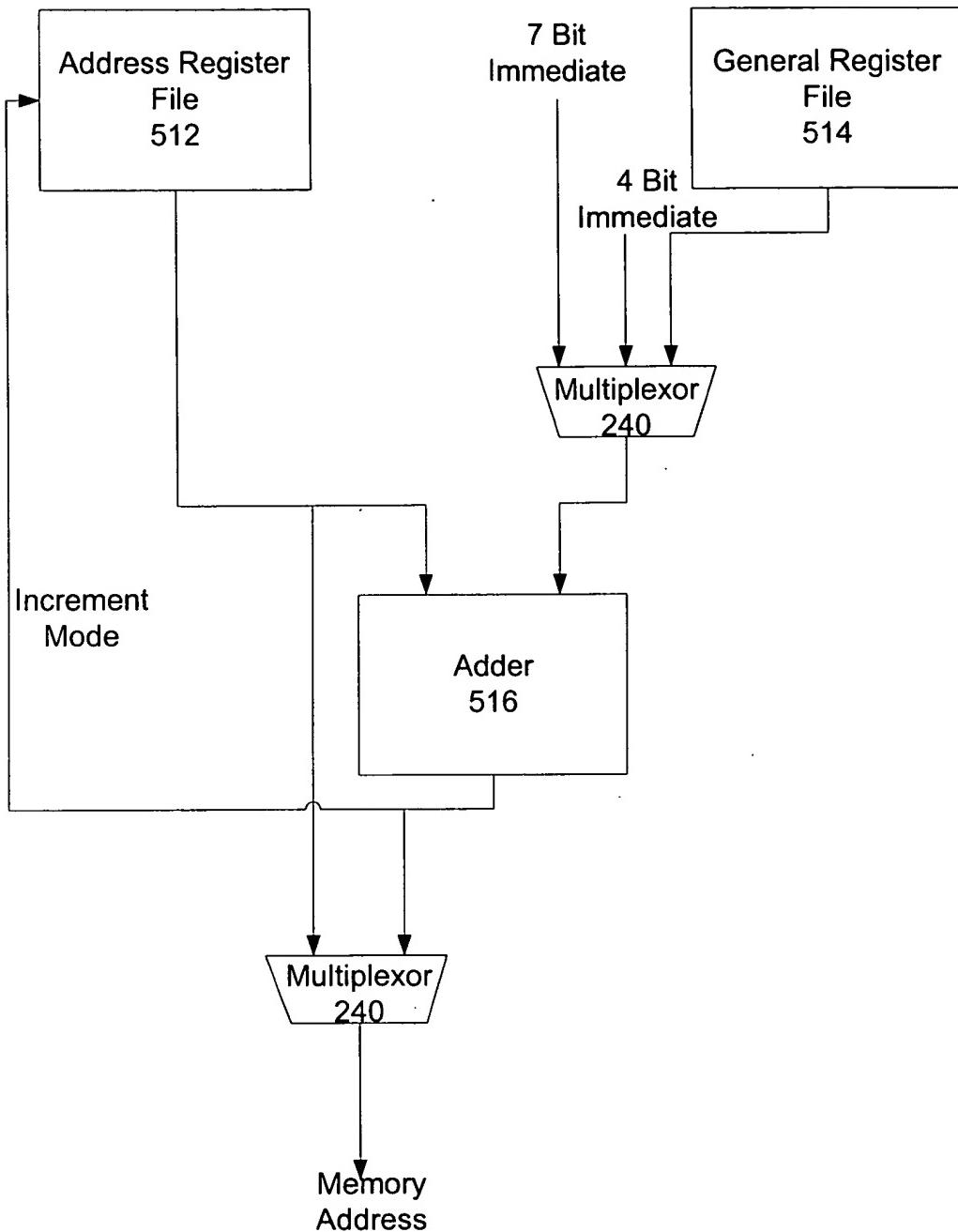


Figure 5

1	I <sub>6</sub>	I <sub>5</sub>	A <sub>2</sub> A <sub>1</sub> A <sub>0</sub>	I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	Row 1			
0	1	1		R <sub>4</sub>	R <sub>3</sub>	R <sub>2</sub>	R <sub>1</sub>	R <sub>0</sub>	Row 2			
0	1	0		M	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	Row 3			
0	0	1		Register Direct								Row 4
0	0	0		Immediate								Row 5

09889295 - 0982204

Figure 6

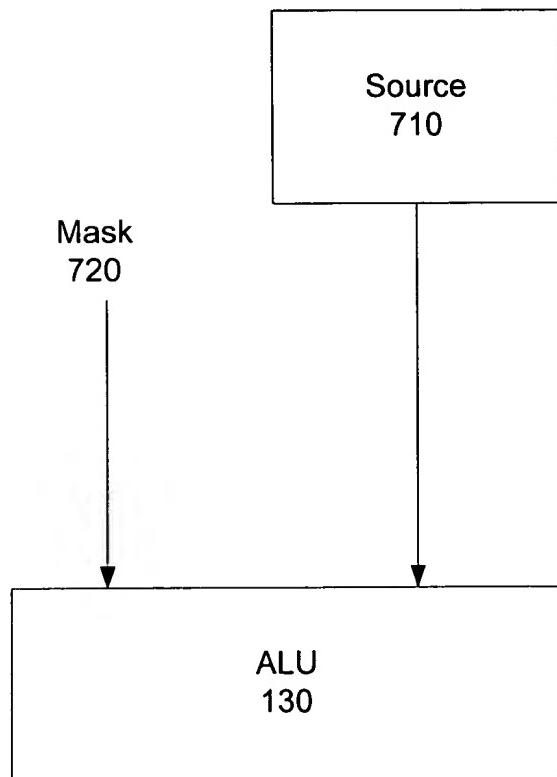


Figure 7

T00369 "5222888888888888"

FIXED LENGTH MEMORY TO MEMORY INSTRUCTION

SET; Inventors: David A. Fctland et.al.;

Docket No.: 20880-06031

Sheet 11

PROCESSED - 05/2002

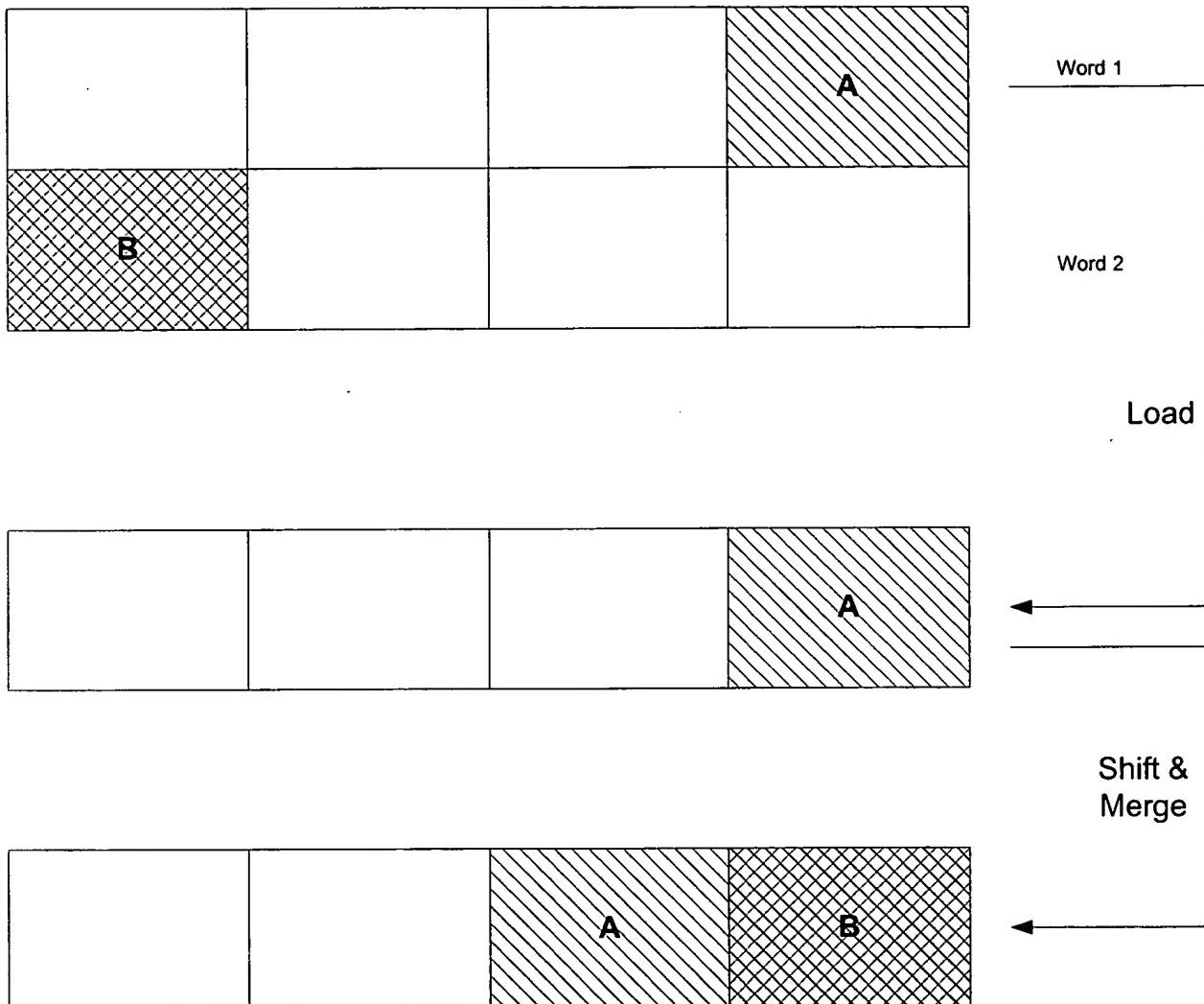


Figure 8

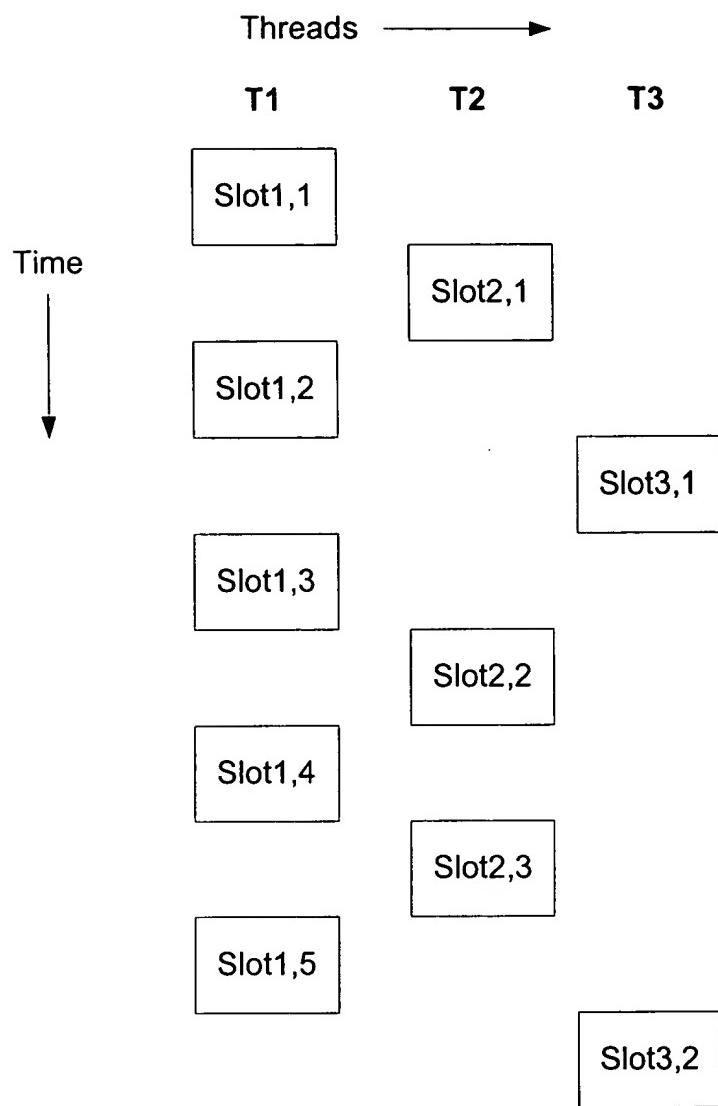


Figure 9